



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,284	02/26/2002	Hyeon-Su An	8028-16 (SPX200110019US)	7098
7590	04/15/2004		EXAMINER	
Frank Chau F.CHAU & ASSOCIATES, LLP Suite 501 1900 Hempstead Turnpike East Meadow, NY 11554			LUU, THANH X	
			ART UNIT	PAPER NUMBER
			2878	
DATE MAILED: 04/15/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/084,284	Applicant(s) AN, HYEON-SU	
	Examiner Thanh X Luu	Art Unit 2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 February 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office Action is in response to amendments and remarks filed February 20, 2004. Claims 1-8 and 10 are currently pending.

#### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4, "the main processor" lacks proper antecedent basis.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 7, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomoyoshi et al. (Japanese Patent 10-318933, published December 4, 1998).

Regarding claims 7, 8 and 10, Tomoyoshi et al. disclose (see Figs. 1 and 3) a multi-functional wafer aligner and method, comprising: a rotatable chuck (23), adapted to receive a semiconductor wafer (W); a wafer transfer unit (not shown), adapted to position the wafer upon the rotatable chuck; a sensor body (at 30), comprising: a position compensator (30); a luminous source (31, 51); and a wafer damage detector

comprising an array of damage-detecting sensors (32a, 32b) to receive light emitted from the luminous source that is reflected off of the edge of the wafer; wherein the sensor body is disposed in relation to the rotatable chuck so as to receive an edge of the wafer within the position compensator. Tomoyoshi further discloses (see Fig. 3) a photodetector (52) disposed upon an opposing side of the luminous source, the photodetector adapted to receive light emitted by the luminous source, wherein the photodetector determines a position of the wafer.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomoyoshi.

Regarding claims 1, 5 and 6, Tomoyoshi discloses (see Figs 1 and 3) a multi-functional wafer aligner, comprising: a multi-functional unit for performing a wafer damage detection; the unit comprising: a wafer rotator (23); an array of luminous emitters (31, 51) for emitting incident rays towards a wafer (W) disposed on the wafer rotator; and an array of damage-detecting sensors (32a, 32b) for receiving the incident rays reflected from the edges of the wafer to detect wafer damage; and a processor (40) for determining positions (with 52) based on a signal. Tomoyoshi also discloses (see Fig. 2) a first area (32a) in the array receives reflected rays when the wafer is not

damaged and a second area (32b) in the array that receives reflected rays when the wafer is damaged. Tomoyoshi does not specifically disclose a flat zone alignment, wafer centering or an accumulated digital signal. However, it is notoriously well known in the art to center a wafer before rotating and detect a flat zone for alignment purposes. Further, it is well known that digital processors are more robust to noise than analog devices. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide an accumulated digital signal, provide flat zone alignment and center the wafer in the apparatus of Tomoyoshi to provide proper alignment for the wafer and to obtain improved operation through more noise resilient digital signals.

Regarding claims 2 and 3, Tomoyoshi discloses (see Fig. 3) a photo detecting sensor (52) for detecting the position of the wafer as claimed. Tomoyoshi does not specifically disclose an array of photodetectors. However, it is a matter of design choice to provide a plurality of detectors. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide an array of photo detecting sensors in the apparatus of Tomoyoshi to provide more precise position signals of the wafer for improved operation.

Regarding claim 4, Tomoyoshi discloses the claimed invention as set forth above. Tomoyoshi does not specifically disclose an alarm. However, it is notoriously well known in the art to create an alarm when a damage condition is present. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention

was made to provide an alarm in the apparatus of Tomoyoshi to alert a user of potential damage to a wafer and improve inspection.

***Response to Arguments***

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X Luu whose telephone number is (571) 272-2441. The examiner can normally be reached on M-F (6:30-4:00) First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Thanh X Luu  
Primary Examiner  
Art Unit 2878